AMENDMENT TO THE DRAWINGS

Applicants submit a sheet of drawings including an amendment to Figure 1. The replacement sheet is submitted to comply with the Examiner's request to designate Figure 1 as Prior Art.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

In this response to the above identified Office Action, Applicants respectfully request reconsideration in view of the above amendments and the following remarks. Claims 1, 5, 6, 11, 14, 17, 20, 22, 25, and 28 have been amended. Claims 4, 7, 23, and 29 have been cancelled. New claims 30 and 31 have been added. Accordingly, claims 1-3, 5, 6, 8-11, 13, 14, 16-20, 22, 24-28, 30, and 31 are pending in the application.

I. Interview Summary

The Applicant's attorney. Jonathan Miller, spoke with the Examiner on October 2, 2007 regarding the Notice of Non-Compliance. The Applicant's attorney requested clarification of the basis for the Notice of Non-Compliance and indicated that it appeared that the previous response met the requirements of 37 CFR § 1.111. The Examiner indicated that he would withdraw the Notice of Non-Compliance and requested that an interview summary be filed by Applicants. Also, an error in claims 5 and 6 was noted by the Examiner.

Applicants resubmit the previous response with the requested interview summary and have also corrected the dependancy issue in claims 5 and 6. Accordingly, it is requested that the Notice Non-Compliance be withdrawn and the response considered.

II. Claim Amendments

Claims 1, 14, 17, 22, 25, and 28 have been amended to include the limitation of "generating a second code as a single program based on the first code" (emphasis added). Support for these amendments may be found in the specification at paragraphs 0023-0030.

Claims 5 and 6 have been amended to clarify the meaning of the claims.

Claims 11 and 20 have been amended to correct a grammatical error.

III. Claims Rejected Under 35 U.S.C. § 112

Claims 3, 5, 6, 19 and 27 stand rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. Examiner states that original claims 1, 17, and 25, from which claims 3-6, 19, and 27 depend, respectively, did not include the limitation of "a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code." Examiner further states that

Applicant's original disclosure does not support an embodiment in which Applicants analyze compiled code and generate "a second code based on the first code, the second code including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code." Hence, Examiner considers the substance of the claims to be new matter. Applicants respectfully disagree.

Referring to Fig. 1, the specification at paragraph 0023 discusses a compiler that converts a source program into macroinstructions (compiled code; *see* Specification, at paragraph 0004). In paragraphs 0024 and 0025, the specification states that the compiler may "perform[] one or more code optimizations" by, for example, converting "the macroinstructions . . . into . . . microinstructions . . . [that] are highly ISA implementation-specific." (*See also* Specification, at paragraph 0006.) Paragraphs 0026 and 0027, however, explain that it is undesirable for a compiled program to consist of only microinstructions, and that, therefore, compilers often do not introduce microinstructions into a compiled program. (*See also* Specification, at paragraph 0005.) Hence, in the present invention, an intermediate code format including a hybrid of macroinstructions and microinstructions is produced. (Specification, at paragraph 0028, and illustrated in Fig. 2.) It is thus disclosed here an embodiment in which compiled code (e.g., the macroinstructions) is analyzed (e.g., in the optimization process), from which a second code (e.g., the intermediate code) including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code, is generated.

Therefore, Applicant's original disclosure supports an embodiment in which Applicants analyze compiled code and generate "a second code based on the first code, the second code including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code." It follows that the substance of the claims does not constitute new matter. Accordingly, reconsideration and withdrawal of the § 112 rejection are requested.

IV. Objections to the Drawings

Fig. 1 stands objected to as not being designated as prior art in the drawings. Applicants submit a corrected replacement sheet. Accordingly, reconsideration and withdrawal of the objection are requested.

The drawings stand objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims. For the reasons discussed above in regard to the § 112 rejection, Applicants respectfully submit that Figs. 1 and 2 illustrate the analysis of compiled code and generation of "a second code based on the first code, the second code including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code." Accordingly, reconsideration and withdrawal of the objection are requested.

V. Claims Rejected Under 35 U.S.C § 102(b)

Claims 1-3, 5, 6, 8-11, 13, 14, 16-20, 22, and 24-28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Slegel et al., "IBM's S/390 G5 Microprocessor Design", IEEE Micro, March/April 1999, Vol. 19, Iss. 2, pp. 12-23 (hereinafter "Slegel"). Applicants respectfully disagree for the following reasons.

To anticipate a claim, Examiner must show that the cited reference teaches each element of a claim.

Claim 1, as amended, includes "generating a second code as a single program based on the first code, the second code including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code" (emphasis added). Examiner has not relied upon and Applicants are unable to discern any part of Slegel that teaches these elements of the claim. Examiner cites Slegel, at "L1 cache," for teaching that "[t]he L1 cache unit also contains a 32-byte writeable millicode array containing the millicode for the most commonly used ESA/390 instructions implemented in millicode." (Office Action, p. 5.) Examiner asserts that "the millicode array is a microarchitecture representation of ESA/390 (macro) instructions that will also be found in the L1 cache at some point in the execution of a given program and both constitute a portion of the second code generated" (emphasis added). (Office Action, p. 5.) However, the millicode and the ESA/390 instructions found "at some point in the execution" do not together constitute a second code as a single program including both microinstructions and macroinstructions. Thus, Slegel does not teach each of the elements of the claim. Accordingly, reconsideration and withdrawal of the anticipation rejection of this claim are requested.

Independent claims 14, 17, 22, 25, and 28, as amended, include elements analogous to those of claim 1. Thus, for at least the reasons discussed above in regard to claim 1, Slegel does

not teach each of the elements of the claims. Accordingly, reconsideration and withdrawal of the anticipation rejection of these claims are requested.

Claim 8 includes "generating compiled code for a given ISA, the compiled code including a) discrete regions of microarchitecture implementation-specific code bounded by ISA format markers and b) macroinstructions outside the discrete regions" (emphasis added). Applicants do not believe that Slegel teaches these elements of the claim. Examiner cites Slegel, at "Millicode," for teaching a "millicode instruction set consist[ing] of all the ESA/390 hardware instructions plus 102 instructions that only millicode can use" and that "there were either more complex instructions or . . . macroinstructions which would appear in the compiled code with the . . . microinstructions of the ESA/390 instruction set." (Office Action, p. 7.) Examiner asserts that "Applicant is only claiming some parts of the code are microinstructions and some parts are macroinstructions which Slegel must inherently have." (Office Action, p. 7.) Applicants respectfully disagree.

"The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." MPEP, at § 2112(IV), *citing In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993). Further, "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." MPEP, at § 2112(IV), *quoting Ex parte Levy,* 17 USPQ2d 1461, 1464 (B.P.A.I. 1990) (emphasis in original). Thus, should Examiner maintain this rejection, Applicants request that Examiner provide such basis and/or reasoning to support the assertion that the occurrence of discrete regions of code, bounded by ISA format markers, necessarily flows from the teachings of the reference.

Thus, Slegel does not teach each of the elements of the claim. Accordingly, reconsideration and withdrawal of the anticipation rejection of this claim are requested.

Claim 11, as amended, includes "a decode unit, the microprocessor having first and second modes of operation, wherein in the first mode, the decode unit decodes ISA format instructions supplied by the fetch unit, and in the second mode, the decode unit processes microarchitecture implementation-specific format instructions supplied by the fetch unit and the microprocessor transitions between the first and second modes upon detection by the decode unit of an ISA format boundary marker supplied by the fetch unit, both the ISA format instructions

and the microarchitecture implementation-specific format instructions being within a same sequence of instructions when supplied by the fetch unit." Applicants do not believe that Slegel teaches these elements of the claim. Examiner refers to paragraph 15 of the Office Action, in the rejection of claim 11. (Office Action, p. 7.) However, paragraph 15 states only that "[a]s to claim 7, Slegel taught: 'the method of claim 1, wherein the alternative representation comprises microcode (fourth paragraph of Microarchitecture section).'" (Office Action, p. 6.) Applicants are unable to discern any part of the cited section that teaches the elements of claim 11. Thus, Slegel does not teach each of the elements of the claim. Accordingly, reconsideration and withdrawal of the anticipation rejection of this claim are requested.

Independent claim 20, as amended, includes elements analogous to those of claim 11. Thus, for at least the reasons discussed above in regard to claim 11, Slegel does not teach each of the elements of the claim. Accordingly, reconsideration and withdrawal of the anticipation rejection of the claim are requested.

Claims 2, 3, 5, 6, 9, 10, 13, 16, 18, 19, 24, 26, and 27 depend from independent claims 1, 8, 11, 14, 17, 20, 22, 25, and 28, respectively, and incorporate the limitations thereof. Thus, for at least the reasons discussed above in regard to the independent claims, Slegel does not teach each of the elements of these claims. Accordingly, reconsideration and withdrawal of the anticipation rejection of the claim are requested.

VI. New Claims

Applicants have added new independent claim 30. Support for this claim may be found in the specification at paragraphs 0023-0028 and Figs. 1 and 2. Applicants have added new claim 31, which depends from claim 30. Support for this claim may be found in the specification at paragraphs 0031-0035 and Figs. 3 and 4.

New claim 30 includes "optimizing the first compiled code into a second compiled code, the second compiled code including a macroinstruction segment and microinstruction segment, the microinstruction segment representing an alternate implementation of a function of the macroinstruction segment; storing the second compiled code as a single compiled program." Applicants are unable to discern any part of Slegel that teaches these elements of the claim. Thus, Applicants submit that this claim is patentable over Slegel.

New claim 31 depends from new independent claim 30, and incorporates the limitations thereof. Thus, for reasons discussed above in regard to the independent claim, Applicants submit that claim 31 is also patentable over Slegel.

CONCLUSION

In view of the foregoing, the Applicants believe that all claims are now in condition for allowance and the Applicants earnestly solicit such action at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/10, 2007

Jonathan S. Miller Reg. No. 48,534

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(310) 207-3800

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on 10-10, 2007.

Melissa Stead 10-10, 2007